interface intf();

logic hclk;

logic hresetn;

logic enable;

logic [31:0] dina;

logic [31:0] dinb;

logic [31:0] addr;

logic wr;

logic [1:0] slave\_sel;

logic [31:0] dout;

clocking dri\_cb@(posedge hclk);

output hclk;

output hresetn;

output enable;

output dina;

output dinb;

output addr;

output wr;

output slave\_sel;

input dout;

endclocking

clocking mon\_cb@(posedge hclk);

input hclk;

input hresetn;

input enable;

input dina;

input dinb;

input addr;

input wr;

input slave\_sel;

input dout;

endclocking

endinterface